CLAIMS

What is claimed is:

1. A generator of a pulse width modulated signal, comprising:

a generator of a sawtooth signal;

a generator of high and low reference signals defining, based on a set-point signal, a linear range of each ramp of the sawtooth signal;

a comparison element configured to compare the sawtooth signal with each of the reference signals and produce comparison signals associated, respectively, with the reference signals; and

a logic combination element configured to combine the comparison signals, thereby providing said pulse width modulated signal.

2. The generator of claim 1 wherein said high and low reference signals are symmetrical with respect to a predetermined value.

3. The generator of claim 2 wherein the predetermined value is equal to half of a maximum voltage value reached by the sawtooth signal.

4. The generator of claim 1 wherein the sawtooth signal is of fixed frequency and amplitude.

5. The generator of claim 1, further comprising an RS-type flip-flop having a first input receiving the pulse width modulated signal of said combination element and a second input directly receiving one of the comparison signals provided by said comparison element.

6. The generator of claim 5 wherein the first input is the set input and the second input is the reset input.

7. The generator of claim 1 wherein said logic combination element comprises an XOR-type gate or an AND-type gate.

8. The generator of claim 1 wherein the generator of the reference signals comprises an input stage receiving said set-point signal and controlling a current mirror having an output terminal providing said reference signals.

9. The generator of claim 8 wherein said reference signals are symmetrical with respect to a predetermined valve and the current mirror comprises:

an input branch formed of a series connection, between high supply and reference rails, of a first PNP-type bipolar transistor and of a first NPN-type transistor, the base of the PNP-type transistor being interconnected to its collector; and

said output branch which comprises a series connection, between said high and reference rails, of a second PNP-type transistor having its collector providing the high reference signal, of two resistors, and of a second NPN-type transistor having its collector providing the low reference signal, the bases of the first and second PNP-type transistors being interconnected, the junction point of said resistors being connected to the output of an operational amplifier having a non-inverting input receiving said predetermined value, and having an inverting input interconnected to its output.

10. The generator of claim 5 wherein said set-point signal is a regulation signal.

11. A DC/DC voltage converter, of voltage step-up or step-down type, comprising :

a generator of a pulse width modulated signal, including:

a generator of a sawtooth signal;

a generator of high and low reference signals defining, based on a set-point signal, a linear range of each ramp of the sawtooth signal;

a comparison element configured to compare the sawtooth signal with each of the reference signals and produce comparison signals associated, respectively, with the reference signals; and

a logic combination element configured to combine the comparison signals, thereby providing said pulse width modulated signal.

12. A method for generating a pulse width modulated signal at a selected frequency, comprising:

generating a sawtooth signal at the selected frequency;

generating high and low reference signals having a voltage difference related to a modulating input level;

comparing the high reference signal to the sawtooth signal to produce a first comparison signal;

comparing the low reference signal to the sawtooth signal to produce a second comparison signal; and

combining the first and second comparison signals to produce the pulse width modulated signal.

13. The method of claim 12 wherein the generating the high and low reference signals comprises:

generating a fixed reference signal of a selected value;

generating the high and low reference signals symmetrically above and below the fixed reference signal, respectively.

14. The method of claim 13 wherein the value of the fixed reference signal is selected to be approximately half a maximum value of the sawtooth signal.

15. The method of claim 12 wherein the combining step comprises establishing the width of a given pulse of the pulse width modulated signal by beginning the given pulse at a crossing of the sawtooth signal and the low reference signal and ending the given pulse at a crossing of the sawtooth signal and the high reference signal.

16. The method of claim 12 wherein the generating high and low reference signals comprises:

inputting the modulating input to an input branch of a current mirror circuit having the input branch and an output branch, the output branch including first and second resistors coupled in series at respective first terminals and defining therebetween a reference node;

inputting a fixed reference value to the reference node; and

outputting the high and low reference signals from respective second terminals of the first and second resistors.

17. A device, comprising:

means for generating a sawtooth signal;

means for generating high and low reference signals having a voltage difference related to a modulating input level;

means for comparing the high reference signal to the sawtooth signal to produce a first comparison signal;

means for comparing the low reference signal to the sawtooth signal to produce a second comparison signal;

means for combining the first and second comparison signals to produce a pulse width modulated signal.

18. A device, comprising:

a generator configured to produce a sawtooth signal;

a generator configured to produce high and low reference signals having between them a voltage difference related to a modulating input level;

a circuit configured to compare the high reference signal to the sawtooth signal to produce a first comparison signal;

a circuit configured to compare the low reference signal to the sawtooth signal to produce a second comparison signal; and

a logic circuit configured to combine the first and second comparison signals to produce the pulse width modulated signal.

19. of claim 18 wherein the high and low reference signals are equally spaced, respectively, above and below a value midpoint between maximum and minimum values of the sawtooth signal.